SYMBOL TIMING CORRECTION FOR A PHASE MODULATED SIGNAL WITH MUTUALLY INTERFERING SYMBOLS

ABSTRACT OF THE DISCLOSURE

A circuit and method for correcting timing of a received phase modulated signal. The method uses k most recently received data bits as an address for a lookup table 60. The lookup table includes reconstructed waveforms from which a timing weighing factor is determined. The received PM from time t_1 is delayed, phase adjusted, and multiplied by the timing weighing factor, the product of which is used by a timing adjust block 50 to adjust timing of the PM signal at a time after t_1. The circuit inputs a PM signal to a timing adjust block 50. The output is split between a matched filter 54 and a loop phase shifter 78. The matched filter feeds alternating I and Q bits into a register 58 that holds k data bits, which are used as an address for a lookup table 60. The output of the lookup table 60 becomes a timing weighing figure, which is multiplied 74 with an output of the loop phase shifter 78 and then input into the timing adjust block 50 for adjusting timing of a PM signal. Phase error may be corrected with minor additional components.